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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,584	03/09/2006	Toshiharu Takayama	24530-009/MXM	9041

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1133 AVENUE OF THE AMERICAS
NEW YORK, NY 10036

EXAMINER

STARK, JARRETT J

ART UNIT	PAPER NUMBER
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2823

MAIL DATE	DELIVERY MODE
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12/02/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/538,584	Applicant(s) TAKAYAMA, TOSHIHARU	
	Examiner JARRETT J. STARK	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 October 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6 and 9-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 6 and 9-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>07/19/2006</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of group II claims 6, 9, 10 and 11 in the reply filed on 10/8/2008 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

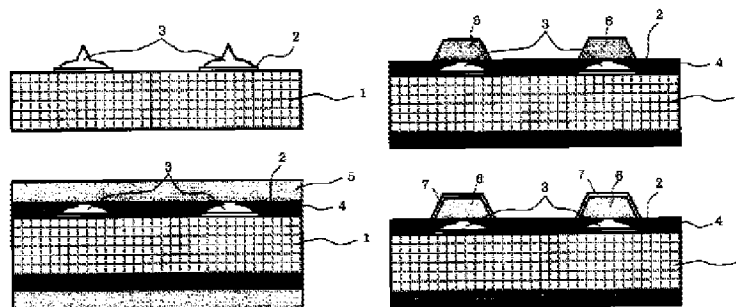
A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 6, 9, and 10 are rejected under 35 U.S.C. 102(a) as being anticipated by Naoto (PAJ 2002-033414).

【図1】



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BASIC-ABSTRACT:

NOVELTY - Metal bump (3) with strap edge for bonding wire, is formed on an aluminum or copper electrode (2) on a semiconductor wafer (1). A copper laminate (5) comprising resin layer is formed over the pressed bump and is etched to form copper electrode (6) on the bumps. Non-electrolytic nickel plating and gliding (7) is provided to the copper electrode.

Regarding claim 6, Naoto discloses the method for producing a flip-chip mounting electronic component having a plurality of terminals [3]/[2] dotted on a mounting face [1] and a plurality of conductors [6] formed on the terminals, comprising the steps of:

coating the mounting face with a conductor having a predetermined thickness (layer [5]);

masking corresponding positions for the terminal parts on the conductor surface (Abstract); and

removing the conductor except the mask parts (copper layer [5] is masked and etched to form copper conductor [6]),

the coating, masking and removing steps being carried out in the stated order (see progression of drawings depicted in provided figure 1).

Regarding claim 9, Naoto discloses the method for producing a circuit board having a plurality of flip-chip mounting lands dotted on a mounting face (Fig. 1), comprising the steps of:

coating the mounting face with a conductor [5] having a predetermined thickness;

masking corresponding positions for the lands on the conductor surface (Abstract); and

removing the conductor except the mask parts (see progression of layer [5] to conductors [6]), the coating, masking and removing steps being carried out in the stated order (Fig. 1).

Regarding claim 10, Naoto discloses the method for producing a package in which mounting face terminal parts of a flip-chip mounting electronic component and/or flip-chip mounting lands of a circuit board mounting face have conductors (Fig. 1), the method comprising:

forming the conductors as remaining parts from growing formation and/or removal (Fig. 1); and

securing the conductors of the circuit board and the electronic component or the conductors of the electronic component and the circuit board with solder or anisotropic conductive material (Entire document – this limitation is the implicit understood conventional use of the known bump terminal structure).

Claims 6, 9, 10 and 11 rejected under 35 U.S.C. 102(e) as being anticipated by Sugihara (US 6,406,991 B2).

Regarding claims 6, 9 and 10, Naoto discloses the method for producing a package in which mounting face terminal parts of a flip-chip mounting electronic component and/or flip-chip mounting lands of a circuit board mounting face have conductors (Figs. 5A-G), the method comprising:

forming the conductors as remaining parts from growing formation and/or removal (Figs. 5A-G); and

securing the conductors of the circuit board and the electronic component or the conductors of the electronic component and the circuit board with solder or anisotropic conductive material (Col. 23&24 – this limitation is the implicit understood conventional use of the device).

Regarding claim 11, Naoto discloses the method for producing a package according to claim 10, wherein the conductors are constituted of copper and on surfaces thereof a nickel layer and a gold layer are formed in the stated order (Figs. 5A-G), and securing step is carried out by fixing force of solder (Col. 23&24).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARRETT J. STARK whose telephone

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number is (571)272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

11/26/2008

/Jarrett J Stark/

Examiner, Art Unit 2823